## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant

: Bedichek, et al.

Confirmation No.: 7303

Serial No.

: 09/417,332

Group Art Unit: 2183

Filed

: 10/13/1999

Examiner: Ellis, R.

For

: METHOD FOR INTEGRATION OF INTERPRETATION AND

TRANSLATION IN A MICROPROCESSOR

## RESPONSE TO NOTICE OF ALLOWANCE

Commissioner for Patents & Trademarks Washington, D.C. 20231

Sir:

Please find herein a certification statement for the above referenced case which supersedes the certification statement filed with the information disclosure statement (IDS) filed on 5/24/2010. Please also find a copy of the Electronic Patent Application Fee Transmittal that accompanied the IDS filed on 5/24/2010. Note that the IDS was filed in conjunction with an Issue Fee payment.

TRAN-P009 Serial No. 09/417,332 Page 1

Examiner: Ellis, R. Group Art Unit: 2183

## **CONCLUSION**

Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,

MURABITO, HAO & BARNES, LLP

Dated: May 26, 2010

/Anthony C. Murabito/

Anthony C. Murabito Registration No. 35,295

Two North Market Street Third Floor San Jose, CA 95113 (408) 938-9060

Page 2

Examiner: Ellis, R. Group Art Unit: 2183